

Customer No.: 31561
Docket No.: 7558-US-PA
Application No.: 10/064,916

AMENDMENTS

Please amend the application as indicated hereafter.

To the Claims

1. (previously presented) A multi-memory architecture with an externally accessible storage capacity known as a total memory capacity and a number of pins of the multi-memory architecture having the total memory capacity known as a total pin number, wherein the total pin number comprises used and unused pins, the multi-memory architecture comprising: a first type non-volatile memory device having a first data storage capacity and a first predefined pin configuration having a first number of pins which is an actual number of used pins according to the first data storage capacity; and

a second type non-volatile memory device having a second data storage capacity and a second predefined pin configuration having a second number of pins which is an actual number of pins according to the second data storage capacity; wherein the first number of pins is greater than the second number of pins, the total pin number of the multi-memory architecture is equal to the number of pins of the first type non-volatile memory device of the multi-memory architecture and the first type non-volatile memory device and the second type non-volatile memory device are disposed in the multi-memory architecture at the same time.

2. (previously presented) The multi-memory architecture of claim 1, wherein the total memory capacity is equal to the first data storage capacity plus the second data storage capacity.

3. (previously presented) The multi-memory architecture of claim 1, wherein the second type non-volatile memory device comprises a plurality of segments and each segment has

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a data storage capacity equal to the first data storage capacity; wherein storage space of the first type non-volatile memory device is used to replace one of the segments in the second type non-volatile memory device so that an access to the replaced segment is mapped to the storage space of the first type non-volatile memory device.

4. (previously presented) The multi-memory architecture of claim 3, wherein the segment in the second type non-volatile memory device that is currently being replaced by the first type non-volatile memory device is used to replace any one of the segments in the second type non-volatile memory device other than the one currently being replaced by the first type non-volatile memory device.

5. (previously presented) The multi-memory architecture of claim 3, further comprising: at least one replacement segment in the second type non-volatile memory device, whose data storage capacity equals the data storage capacity of each segment in the second type non-volatile memory device, is used to replace any one of the segments in the second type non-volatile memory device other than the one being currently replaced by the first type non-volatile memory device.

6. (previously presented) The multi-memory architecture of claim 1, further comprising a replacement memory area in the second type non-volatile memory device, whose data storage capacity equals the first type non-volatile memory device, is used to replace any one of the segments in the second type non-volatile memory device other than the one being currently replaced by the first type non-volatile memory device.

7. (previously presented) The multi-memory architecture of claim 5, wherein one of the

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at least one replacement segment that is currently being replaced by the first type non-volatile memory device, is used to replace any one of the segments in the replacement memory area other than the one currently being replaced by the first type non-volatile memory device.

8-26 (cancelled)